REMARKS

Applicants affirm the provisional election made by Barmak Sani on 5/31/01 of invention I (claims 1 through 29) to be examined. Accordingly, claims 1-29 are pending, and claims 30-36 are withdrawn from further consideration as being drawn to a non-elected invention.

Claims 1, 6, 7, 9, 26, 27, and 28 are amended to more clearly set forth the invention. Claims 19 and 20 are canceled without prejudice, and new claims 37-49 are added. Support for the amended claims and the newly added claims can be found throughout the specification and the drawings.

Page 2 of the specification has been amended to correct two typographical errors in accordance with the Examiner's helpful suggestions. Page 2 is further amended to include reference to element 109 in Fig. 1A to overcome the Examiner's drawings objection.

No new matter is believed added. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made"**.

Drawings objections

Fig. 1A is objected to under 37 CFR 1.84(p)(5) for including element 109 not mentioned in the specification. Page 2 of the specification is amended to include reference to element 109, and accordingly, withdrawal of this objection is respectfully requested.

The drawings are objected to under 37 CFR 1.83(a) for failing to show the features recited in claim 19. Claim 19 has been canceled, and thus the basis for this objection has been eliminated.

Specification objections

Page 2 of the specification is objected to for occurrence of two informalities, namely, typographical errors. Page 2 of the specification is amended to correct the cited informalities, and thus, withdrawal of the this objection is respectfully requested.

Claim rejections

Pending claims 1-4, 7-9, 25, 26 are rejected under 35 USC 102(b) as being anticipated by Kohda et al., USP 5,021,999. Pending claims 5, 6, 21-24, 27-29 are rejected under 35 USC 103(a) as being unpatentable over Kohda et al. in view of Guterman, USP 5,153,691. These rejections are respectfully traversed.

Claim 1, as amended, distinguishes over Kohda et al. and Guterman taken singly or in combination at least by reciting "the select-gate ... extending across the entire length of each of the first and second junctions, and the select gate being separated from the first and second floating gates only by an insulating layer." Support for this feature of applicants' claim 1 can, for example, be found in Figs. 5A and 5B. As shown in both Figs. 5A and 5B, select gate 501 extends horizontally across the entire length of each of the two junctions 504 and 505.

As clearly shown in Figs. 9 and 10 of Kohda et al., control gate 6 extends vertically, and as such does not extend over the drain region 2 and source region 3. Thus, Kohda et al. does not teach or suggest "the select-gate ... extending across the entire length of each of the first and second junctions", as recited in Applicants' claim 1.

Claim 1 distinguishes over Guterman at least by reciting "a cell structure comprising: ... first and second floating gates". Guterman nowhere teaches or suggests such cell structure.

Thus, claim 1 and its dependent claims 2-18, and 21-27 distinguish over Kohda et al. and Guterman taken singly or in combination, and are thus allowable.

Claim 28 includes similar limitations to those of claim 1 recited above, and thus claim 28 and its dependents claim 29 and newly added dependent claim 37 distinguish over Kohda et al. and Guterman for at least the same reasons cited above.

New claims 38-44 distinguish over Kohda et al. and Guterman taken singly or in combination in a number of respects. For example, claim 38 distinguishes over the two references by reciting "a method of operating a memory cell having ... first and second floating gates ..., the method comprising: ... in a first read operation, reading the first bit of data stored in the first floating gate; and in a second read operation, reading the second bit of data stored in the second floating gate."

Kohda et al. disclose a method of operating the memory cell whereby three or more bits of data are stored in a single memory cell (col. 3, lines 14-17). Fig. 5 of Kohda et al. shows a graph of the cell current I_D versus the control gate voltage V_G. Three different I-V curves are shown: line L1 corresponds to an erased cell, line L2 corresponds to the case wherein only one of the two floating gates is programmed, and line L3 corresponds to the case wherein both floating gates are programmed (see col. 7, line 44 to col. 8, lines 18). With three distinct I_D current characteristics and using two reference currents Iref1 and Iref2, "it becomes possible to read out 3-logic level data from the memory cell by comparing the drain current I_D and the reference currents." (col. 8, lines 15-18). Thus, in contrast to Applicants' claim 38 wherein each bit of data stored in the memory cell corresponds to only one of the floating gates, in Kohda et al. each bit of data in the memory cell corresponds to both floating gates.

Claim 38 distinguishes over Guterman because neither the memory cell structure nor the operating method recited in claim 38 is taught or suggested by Guterman.

Thus, claim 38 and its dependent claims 39-45 distinguish over Kohda et al. and Guterman for at least the above-cited reasons.

New claims 46-49 distinguish over Kohda et al. and Guterman taken singly or in combination in a number of respects. For example, claim 46 distinguishes over each of the two references by reciting "changing an electrical potential of the first floating gate by applying a first set of voltages to the select gate, the body region, the drain region, and the source region to induce injection of hot electrons into the first floating gate from the channel region under the source-side of the first floating gate".

As shown in Fig. 4A, Kohda et al. bias the memory cell to change the electrical potential of the right floating gate 4a by applying voltages to the cell terminals to induce injection of hot electrons into the right floating gate 4a from the channel region under the drain-side of the right floating gate 4a, not its source side as recited in Applicants' claim 46.

Claim 46 distinguishes over Guterman because neither the memory cell structure nor the operating method recited in claim 46 is taught or suggested by Guterman.

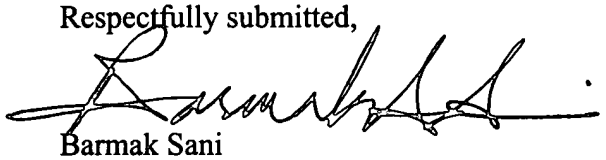
Thus, claim 46 and its dependent claims 47-49 distinguish over Kohda et al. and Guterman for at least the above-cited reasons.

CONCLUSION

In view of the foregoing, Applicants believe that the pending claims 1-18 and 21-29, and the newly added claims 37-49 are in condition for allowance.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Page 2, the paragraph beginning at line 11, has been amended as follows:

A structural difference between cells 100 and 150 is that the **[triply]** triple-polysilicon cell 100 has five operating terminals (select-gate 101, control-gate 102, drain 104, source 105, and substrate 106), while the double-polysilicon cell 150 has four operating terminals (select-gate 151, drain 154, source 155, and substrate 156). Note that drain junction 154 is deeper than source junction 155 to increase floating gate 153 to drain 154 overlap capacitance for improved voltage coupling from the drain to the floating gate. Cell 100 has a channel portion 109.

Page 2, the paragraph beginning at line 22, has been amended as follows:

While the programming mechanisms of cell structures 100 and 150 are similar (e.g., source-side injection, shown by the arrows P in Figs. 1A and 1B), their erase operations differ. In the triple-polysilicon cell 100, during **[ease]** erase, the electrons are tunneled from floating gate 103 to drain 104 via a thin gate-dielectric 107. This is shown by the arrow E in Fig. 1A. However, in the double-polysilicon cell 150, the electrons are tunneled from floating gate 153 to select-gate 151 via a thin inter-polysilicon dielectric 158 at a pointed corner of floating gate 153. This is shown by the arrow E in Fig. 1B.

In the Claims:

Claims 19 and 20 have been canceled. Claims 1, 6, 7, 9, 26, 27 and 28 have been amended as follows:

1. (Amended) A cell structure comprising:

a first junction and a second junction separated by a channel region, the first and second junctions being in a body region, the separation between the first and second junctions defining a cell channel length extending horizontally, each of the first and second junctions having a vertically-extending width, a horizontally-extending length, and a depth;

[a] first and **[a]** second floating gates over the channel region;**[,]** and

a select-gate having a portion between the first and second floating gates, the select-gate also extending over at least a portion of each of the two floating gates and extending across the entire length of each of the first and second junctions, and the select gate being separated from the first and second floating gates only by an insulating layer.

6. (Amended) The cell structure of Claim 5 **[further comprising an inter-polysilicon dielectric layer for insulating the first and second floating gates from the select-gate, the inter-polysilicon dielectric layer being]** wherein the insulating layer is thinnest between the sharp edge of each of the two floating gates and the select-gate.

7. (Amended) The cell structure of Claim 1 wherein each of the first and second floating gates has a vertically-extending width, a horizontally-extending length, and a depth, the select-gate **[extends over and beyond]** extending across the entire length of each of the first and second floating gates.

9. (Amended) The cell structure of Claim 1 wherein each of the first and second floating gates **[is capable of storing]** stores one bit of information.

Cancel claims 19 and 20.

26. (Amended) The cell structure of Claim **[7]** 1 in combination with other similar cell structures forming a virtual ground array of rows and columns of cells, **[wherein]** the cells along each row being **[are]** serially connected **[along a plurality of rows and columns]**, the select-gates of the cells along each row being connected together forming a **[wordline]** plurality of horizontally-extending select-gate lines, the first junction of cells along each column of cells being connected together forming a first plurality of vertically-extending bitlines **[continuous bitline]**, and the second junction of the cells along each column of cells being connected together forming a second plurality of vertically-extending bitlines **[another continuous bitline]**.

27. (Amended) The cell structure of **[c]**Claim 1 **[further comprising an inter-polysilicon dielectric layer for insulating the first and second floating gates from the select-gate, the inter-polysilicon dielectric having]** wherein the insulating layer has a weak region so that electrons can tunnel from the first and second floating gates to the select-gate.

28. (Amended) A memory array comprising:

a plurality of cells arranged to form rows and columns of cells, each cell comprising:

a first junction and a second junction separated by a channel region, the first and second junctions being in a body region, the separation between the first and second junctions defining a cell channel length extending horizontally, each of the first and second junctions having a vertically-extending width, a horizontally-extending length, and a depth;

a first floating gate and second floating gate **[each having at least one slanted surface forming a sharp edge]**, the first floating gate extending over a first portion of the channel region and over a portion of the first junction, and the second floating gate extending over a second portion of the channel region and over a portion of the second junction;

a select-gate extending over **[and beyond]** the two floating gates and extending across the entire length of each of the first and second junctions, the select-gate having a portion between the first and second floating gates, the portion of the select-gate extending over a third portion of the channel region between the first and second channel portions, wherein the first, second, and third portions of the channel region do not overlap and together form the entire channel region;

an inter-polysilicon dielectric layer insulating the first and second floating gates from the select-gate, **[the inter-polysilicon dielectric layer being thinnest between the sharp edge of each of the two floating gates and the select-gate]** the select gate being separated from the first and second floating gates only by said inter-polysilicon dielectric layer; and

a gate-dielectric layer insulating the first and second floating gates and the portion of the select-gate from the underlying channel region and the first and second junctions,

wherein the cells are serially connected along each row, the select-gates of the cells along each row being connected together forming a plurality of horizontally-extending select-gate lines **[wordline]**, the first junction of the cells along each column of cells being connected together forming a first plurality of vertically-extending bitlines **[continuous bitline]**, and the second junction of the cells along each column being connected together forming a second plurality of vertically-extending bitlines **[another continuous bitline]**.